REMARKS

Claims 1-48 are pending and stand rejected. The Examiner's reconsideration of the rejections in view of the following remarks is respectfully requested.

Claims 1-10, 11-19, and 20-29, and 30-39 were rejected under 35 U.S.C. §103(a) over Funk in view of Dias et al. (U.S. Patent 5,010,331). The Examiner stated essentially that Dias teaches a processor connected through N data lines to a "logic unit" and "that there are many more M **data** lines 1.17 (Fig. 1.2) going to the processor 1.14 (Fig. 1.2) than N **data** lines 1.22, 1.26, 1.28 (Fig. 1.2) going to the control logic unit 1.30 (Fig. 1.2)."

As the Examiner acknowledges "Funk et al. fails to clearly teach where M data lines is greater than N data lines", (Office Action, Page 4), Funk (U.S. Patent 6,026,119) does not teach nor suggest a bus data-width change between the processor and the modem, where the modem bus has N data lines while the processor bus has M data lines, where M is greater than N, as claimed in independent claims 1, 11, 21, and 31, and in the claims depending therefrom. Funk teaches only that N is equal to M, and further contains no suggestion nor any motivation to eliminate some (M minus N) data lines from the M = N data communication path "430, 432" between the modem and the processor shown in FIG. 4 of Funk. Instead, Funk equates the M data lines in bus (430) as being the same as the N data lines in bus (432) since Funk characterizes the entire bus "430, 432" between the processor and the "logic unit" (107, Fig. 4) of the RF modem (101) as one single "data and control" bus "430, 432" (see Col. 5, lines 4-7).

Applicant respectfully disagrees with the Examiner's view that Dias teaches

"many more M data lines 1.17 (Fig. 1.2) going to the processor 1.14 (Fig 1.2) than N data lines 1.22, 1.26, 1.28 (Fig. 1.2) going to the control logic unit 1.30 (Fig 1.2)". Dias discloses an external "security key" device to be plugged externally into the "parallel port" of a personal computer, between the computer's parallel port and an external printer. The "parallel port" lines 1.17 are not data lines of a "processor bus" having "M data lines" AND that none of the three (N) lines (1.22. 1.26. 1.28) into the "logic" unit 1.30 of the "security" peripheral 1.10 is a "DATA" line: line 1.22 is "a clock line"; line 1.26 is "a reset-bar line"; and line 1.28 is "a ground line." (Dias, Col. 8, Lines 39-45) None of the supposed "N data lines" in Dias is even a "data line":

> "Connected to the output of the key ring 1.18 is another parallel port connecter 1.19 which in turn is shown connected to a printer 1.20. Connected between the key ring 1.18 and the electronic key 1.10 are four lines: a clock line 1.22, a data line 1.24, a reset-bar line 1.26, and a ground line 1.28." (Dias, Col. 8, Lines 39-45)

The single nominal "data line" 1.24 selected (tapped out) from the "parallel port" lines 1.17 is not connected to the "logic" unit 1.30. A "parallel port" bus is not a "processor bus" having "M data lines". And, three lines of a "parallel port" none of which is a "data line" is not "N <u>data</u> lines". Therefore, Dias does NOT teach a processor bus having address lines and M data lines being reduced or "packed" down into a packet bus (nor any other sort of bus) having fewer (N) "data lines". Thus, neither Funk nor Dias teaches data lines "where M data lines is greater than N data lines" as stated by the Examiner (Page 4 of the Office Action).

Furthermore, the security circuit 1.10 (FIG. 1.2) requiring only one single "data line" selected from a standard "parallel port" interface, does not teach a high-data-volume

peripheral such as a "modem", and thus it does not provide any suggestion or motivation to combine the features of Dias with the circuit of Funk. The one-bit "security key" of Dias is totally dissimilar from the high-data-volume modem of Funk, and there is no motivation to effectively cripple the modem of Funk by employing the one-bit tapping circuit of Dias. Nor does Dias disclose nor suggest a "packet bus" having N data lines configured to be used for conveying high-data-volume (e.g., M-bit wide, Mbs) signals and "control signals". Accordingly, claims 1-10, 11-19, and 20-29, and 30-39 are not rendered obvious over Funk in view of Dias.

With respect to the Examiner's suggestion that "a signal modulator/demodulator, for effecting radio communications, ... connected to a packet bus having N data lines...; and a central processing unit operatively connected to a processor bus including ... M data lines, wherein M is greater than N" is "pretty well known" (Pages 4, 8) the Examiner's attention is respectfully drawn to MPEP sections 1.104 and 2144.03.

> § 1.104 Nature of examination.
> (d) *Citation of references.*
>
> > (2) When a rejection in an application is based on facts within the personal knowledge of an employee of the Office, the data shall be as specific as possible, and the reference must be supported, when called for by the applicant, by the affidavit of such employee, and such affidavit shall be subject to contradiction or explanation by the affidavits of the applicant and other persons.

Thus, Applicant respectfully requests that the Examiner produce an affidavit in support of this contention.

Claims 31, 35-36, 40, and 44-45 were rejected under 35 U.S.C. §102(b) as anticipated by Funk et al., U.S. Patent 6,026,119. The Examiner stated essentially that

Funk teaches all the limitations recited in claims 31, 35-36, including: a "processor bus" having "address lines", a "packet bus" for controlling an RF modem, and a master controller connected to both (between) those two busses, the master controller being provided for issuing "packetized commands" for controlling the modem (or a plurality of peripherals) through the packet bus.

Funk characterizes the processor busses connecting its processor to two other components as "data and control" buses (which include address lines). Funk specifies that the Processor (421, Fig 4) is directly connected to its RAM ("Memory" 419) via "data and control lines (436)" (see Col 4, Lines 52-57), and the examiner essentially concedes that "control lines" include "address lines" (e.g., Final Office Action Page 2, regarding claim 31).

Funk also characterizes the entire bus "430, 432" between the processor and the "logic unit" (107, Fig. 4) of the RF modem (101) as one "data and control" bus "430, 432" (see Col. 5, lines 4-7). Meanwhile, within the same two paragraphs, Funk contradistinguishes and differently characterizes the bus between the processor (421) and the keyboard ("operator interface" 425) as an "Input/Output (I/O) bus" (434). (see Col. 4, lines 57-60).

Thus, Funk teaches that the Processor-Modem bus ("430, 432") is of the same "data and control [i.e., address]" line bus type as the Processor-RAM bus (436), while the "(I/O)"bus (434) to the keyboard ("operator interface" 425) is a different type of bus.

Further, since Funk teaches that each of the Processor-RAM bus (436) and the Processor-Modem bus ("430, 432") contains both dedicated "data" lines and dedicated

"control" lines (i.e., each is a conventional "data and control" processor bus including address lines), Funk does not teach or suggest sending a "packetized command" over the N "data" lines of the Processor-Modem bus ("430, 432").

The Examiner previously referred to all three busses "430, 432 and 434" shown in Fig. 4 of Funk as being "the common bus" (First, Non-Final, Office Action). In the present (Final) Office Action, the Examiner characterizes the bus(ses) differently: "432 and 434" (shown in Fig. 4 of Funk) together as "a processor bus including address lines and M data lines" and at the same time together as "a first packet bus"; the Keyboard bus "430" (shown in Fig. 4 of Funk) as "a second packet bus" (Office Action, Page 2, regarding claim 31); bus 432 alone as being "a processor bus" while characterizing bus "430" alone as "a common bus" (Page 3, regarding claim 40); bus(ses) "430 and 432" together as being "the common bus" (Page 3, concerning claim 44); bus "430" alone as being "a packet bus" ("having N data lines for conveying packetized control and data signals"), and at the same time bus(ses) "432 and 434" (shown in Fig. 4 of Funk) together as "a processor bus including address lines and M data lines" (Pages 4, 5, 8, 9 concerning claims 1, 21, 11, 14 respectively); and all three bus(ses) "430, 432, and 434" together as being "the common bus" (Page 6, concerning claim 25).

The various characterizations of the bus(ses) 430, 432, and 434 (shown in Fig. 4 of Funk) by the Examiner are internally inconsistent. It can be seen that in Funk that neither the Funk "controller" (111, FIG. 4) nor the Funk "logic unit" (107, Fig. 4) is used to "packetize" any "data" nor does either issue "packetized commands" to any of the peripherals (e.g., the RF Modem), since it is explicitly stated in Funk that the PC

processor (421) is what "parse[s] data message into data blocks" making up each "packet" which is/are then conveyed to the "logic unit" (e.g., modem, via a processor bus having address lines). Any "commands" sent by the Funk "controller" (111, FIG. 4) or by the Funk "logic unit" (107) to the "peripherals" (e.g., to the modem) are NOT WITHIN THE DATA "PACKETS" which are generated by the PC "processor". Therefore, such "commands" are not "packetized". Thus, in Funk there is no "packetized command" capable of being "commonly receivable by the plurality of peripherals" [e.g., 101 and 425 (Fig. 4) in Funk] as claimed in claims 35, 44.

Referring to Figs. 5 and 7 and corresponding text in Funk, each so-called "packet (510)" comprises "six-byte transmit data blocks (545-565)" and is, "sent... by the processor (421) to the controller interface (111)" which just passes it along to the logic unit (107). The "controller interface"(111) does not add "packetized commands" to the packet, nor does the "controller interface" (111) create or modify the packets at all. Thus, the "controller interface" (111) does not "issue" "packetized commands" nor does it in any way control any peripheral by issuing "packetized commands" as claimed in claims 5, 14, 25, 35.

See also, Figures 6 and 8 of Funk, neither the "logic unit" (107 in Funk Fig. 4) nor the "Controller interface" (111 in Funk FIG. 4) performs the function of "unpacking" received data "blocks" (or packets) received from the RF modem.

Therefore, Funk does not teach "a packet bus" (distinct from the "processor bus") between the processor (421) and the modem (101), as claimed in claims 1, 11, and 31.

Claims 2-9 depend from claim 1. Claims 12-19 depend from claim 11. Claims 32-39 depend from claim 31. These dependent claims are believed to be allowable for at least the reasons given for claims 1, 11, and 31.

Regarding the Examiner's rejection of claims 40-48, the Examiner states that "peripherals operatively connected to the ... bus" are not necessarily "***on*** the ... bus". [Page 20 of Office Action]. The limitations of claim 40 include "a common bus operatively connected to the master controller and to each of the plurality of peripherals." Applicant believes that "operatively connected" is synonymous with "on the bus". Withdrawal of the rejection is respectfully requested.

As previously noted, dependent claims 44-46 are additionally allowable because there is no suggestion in Funk that any "packetized commands" or "packetized control signals" are issued or conveyed to the plurality of peripherals over the "data and control" bus 430 (including data, address, and control lines) identified by the Examiner (Page 3, regarding claim 40) as being the "common bus" in claim 40.

Applicants respectfully request that the Examiner withdraw the "Final" status of the Office Action to the extent that rejections of the pending claims (e.g., 1-10, 11-19, and 20-29, and 30-39) are based upon Funk "in view of Dias" (i.e., a combination with Dias et. als. U.S. Patent 5,010,331), since neither Dias nor Funk et al. (U.S. Patent 6,026,119) teaches or suggests an RF modem on or operatively connected to a (packet) bus having N data lines (N being less than the data width M of the processor's Data/Address line bus).

For the forgoing reasons, the application, including claims 1-48, is believed to be in condition for allowance. Early and favorable action is respectfully urged.

Respectfully submitted,

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